1. A method for communicating between a plurality of asynchronous transmitting and receiving systems using digital streams arranged in multiple access frames, the method comprising:

(a) in a master system, cycling a counter using a clock reference to generate a master count, and using the master count to establish a master frame count;

(b) in a slave system, cycling a counter using a clock reference to generate a main count, and using the main count to establish a main frame count;

(c) from a difference between the master frame count and the main frame count of the slave system, determining a frame count offset value;

(d) establishing a slave frame count for the slave system by adding the offset value to the main frame count, and thereby aligning the slave frame count of the slave system with the master frame count and incrementing the slave frame count when the main count is incremented;

(e) communicating digital streams between the master and slave systems by aligning frames with the clock reference of the master system when the slave frame count for the slave system is aligned with the master frame count.

2. The method of claim 1, wherein the master and slave systems each generate a count with a plurality of bits which define frame boundaries for the respective systems, the step of aligning frames with the clock reference of the master system further comprising determining a bit offset between a master system frame boundary and a slave system frame boundary and adjusting the slave system frame boundary with the bit offset so that the frames are aligned.

3. The method of claim 2 wherein said plurality of bits defining the master frame boundary is a portion of the master count.

4. The method of claim 2 wherein said plurality of bits defining the slave frame boundary is a portion of the slave count.

5. The method of claim 2 wherein said at least one of said master and main counts includes first and second pluralities of bits, the first plurality of bits forming said frame count and the second plurality of bits forming a bit count for defining frame boundaries for the respective systems.

6. The method of claim 1 further comprising generating a bit count for the slave system reflective of the frame boundary of the slave system.

7. The method of claim 6, further comprising:

(a) starting a packet count for each frame of each digital stream using the bit count determined for the frame boundary of the slave system; and

(b) incrementing the packet count at a predetermined rate thereafter for communicating the frame between the systems.

8. The method of claim 2 further comprising monitoring drift between the clock reference of the master system and the clock reference of the slave system and adjusting the bit offset and the slave system frame boundary to reflect the drift between the clock references.

9. The method of claim 1 further comprising monitoring drift between the clock reference of the master system and the clock reference of the slave system and adjusting the slave frame count of the slave system to reflect the drift between the clock references.

10. A communication system including a plurality of asynchronous transmitting and receiving systems using digital streams arranged in multiple access frames, the system comprising:
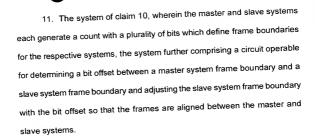
a master system operable for cycling a counter using a clock reference to generate a master count, the master system using the master count to establish a master frame count;

a slave system operable for cycling a counter using a clock reference to generate a main count, the slave system using the main count to establish a main frame count;

a circuit operable for determining a difference between the master frame count and the main frame count and creating a frame count offset value;

the slave system further operable for establishing a slave frame count by adding the offset value to the main frame count, and thereby aligning the master frame count with the main frame count of the slave system, the slave system incrementing the slave frame count when the main count is incremented;

the master and slave systems operable for communicating digital streams therebetween by aligning frames with the clock reference of the master system when the slave frame count for the slave system is aligned with the master frame count.

11. The system of claim 10, wherein the master and slave systems each generate a count with a plurality of bits which define frame boundaries for the respective systems, the system further comprising a circuit operable for determining a bit offset between a master system frame boundary and a slave system frame boundary and adjusting the slave system frame boundary with the bit offset so that the frames are aligned between the master and slave systems.

12. The system of claim 10 wherein said circuit for determining a difference between the master and slave frame counts is part of the slave system.

13. The system of claim 11 wherein said circuit for determining a bit offset between the master and slave system frame boundaries is part of the slave system.

14. The system of claim 11 wherein said plurality of bits defining the master frame boundary is a portion of the master count.

15. The system of claim 11 wherein said plurality of bits defining the slave frame boundary is a portion of the slave count.

16. The system of claim 11 wherein at least one of said master and main counts includes first and second pluralities of bits, the first plurality of

bits forming said frame count and the second plurality of bits forming a bit count for defining frame boundaries for the respective systems.

17. The system of claim 10 wherein said slave system is operable for generating a bit count reflective of the frame boundary of the slave system.

18. The system of claim 17 further comprising a circuit operable for starting a packet count for each frame of each digital stream using the bit count determined for the frame boundary of the slave system, the packet count being incremented at a predetermined rate thereafter for communicating the frame between the systems.

19. The system of claim 11 further comprising a circuit operable for monitoring drift between the clock reference of the master system and the clock reference of the slave system and adjusting the bit offset and the slave system frame boundary to reflect the drift between the clock references.

20. The system of claim 10 further comprising a circuit operable for monitoring drift between the clock reference of the master system and the clock reference of the slave system and adjusting the slave frame count of the slave system to reflect the drift between the clock references.